ABSTRACT

Multi-gate MOS transistors and fabrication methods are described, in which the transistor semiconductor body thickness or width is lithography independent, allowing scaled triple and quad-gate devices having semiconductor bodies smaller than a lateral gate length dimension. A form structure is provided over a semiconductor wafer starting structure, and spacers are formed along one or more sidewalls of an opening in the form structure. A semiconductor material is deposited in the opening by epitaxial growth or other deposition process, and the form structure and the spacer are removed. A gate structure is then formed along the top and sides of a central portion of the formed semiconductor body. The spacer may be L-shaped, providing an undercut or recess at the bottom of the semiconductor body sidewall, and the gate may be formed in the undercut area to allow fabrication of more than three gates.